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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,244	02/17/2004	Seong-Jun Heo	5649-1191	9666

20792 7590 06/16/2005

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EXAMINER	
FORDE, REMMON R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,244	HEO ET AL.	
	Examiner	Art Unit	
	Remmon R. Fordé	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,7,10-18,24 and 25* is/are rejected.

7)☒ Claim(s) *2,5,6,8,9 and 19-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/4/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response To Election

The Examiner hereby acknowledges Applicant's election of claims 1-25 in correspondence dated 03/22/2005.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10, 11 and 14-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 10, line 1, phrase "the barrier metal layer" lacks proper antecedent basis.

In claim 11, line 2, phrase "the barrier metal layer" lacks proper antecedent basis.

In claim 14, line 2, phrase "the semiconductor substrate" lacks proper antecedent basis.

In claim 15, line 2, phrase "the semiconductor substrate" lacks proper antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 7, 12-18, 24 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al..

Regarding claim 1, referencing Figures 4A-4E, Chen et al. discloses a method of manufacturing a MOS device provided with the steps of: patterning a metal-gate layer (24) and a gate polysilicon layer (23) to form a gate pattern comprising a gate polysilicon pattern (23) and a metal-gate pattern (24); and covering at least a portion of a sidewall of the metal-gate pattern with an oxidation barrier layer (29), wherein the oxidation barrier layer comprises metal (i.e. titanium). (Column 2, line 57 – Column 3, line 47.)

Regarding claim 3, referencing Figures 4A-4E, Chen et al. further discloses that the oxidation barrier layer (29) comprises an oxide of a metal (i.e. titanium oxide). (Column 3, lines 26-38.)

Regarding claim 4, referencing Figures 4A-4E, Chen et al. further discloses, as previously stated above, that the oxidation barrier layer contains the metal of titanium. (Column 3, lines 26-38.)

Regarding claim 7, referencing Figures 4A-4E, Chen et al. further discloses that the oxidation barrier layer has a thickness of between about 5 ~100 Angstroms. (Column 3, lines 25-32.)

Regarding claim 12, referencing Figures 4A-4E, Chen et al. further discloses forming a capping layer (25) on the metal-gate layer (24), wherein the capping layer is patterned when the metal-gate layer (24) and the gate polysilicon layer (23) are sequentially patterned, thereby forming a stacked gate pattern comprising, in serial order, a gate polysilicon pattern (23), a metal-gate pattern (24) and a capping pattern (25). (Column 3, lines 1-19.)

Regarding claim 13, referencing Figures 4A-4E, Chen et al. further discloses forming a spacer layer (28) to substantially cover a sidewall of the gate pattern including: the sidewalls of the polysilicon pattern; the oxidation barrier layer; and the sidewalls of the capping pattern. (Column 3, lines 47-52.)

Regarding claim 14, insofar as understood, referencing Figures 4A-4E, Chen et al. further discloses forming an impurity-doped region (27) in a semiconductor substrate (20) at opposing sides of the gate pattern using the gate pattern as an ion-implantation mask. (Column 3, line 47 – Column 4, line 7.)

Regarding claims 15 and 16, insofar as understood, referencing Figures 4A-4E, Chen et al. further discloses thermally treating the semiconductor substrate having the gate pattern with the oxidation barrier layer under an oxygen-enriched environment. (Column 4, lines 8-17.)

Regarding claims 17 and 18, referencing Figures 4A-4E, Chen et al. further discloses a method of manufacturing a MOS device having a metal gate electrode provided with the steps of: forming a stacked gate pattern onto a target substrate (20), the gate pattern comprising a metal-gate pattern (24) with opposing first and second surfaces and at least one sidewall; and covering at least a portion of the at least one sidewall of the metal-gate pattern (24) with an oxidation barrier layer (29) substantially without covering a sidewall of an adjacent gate polysilicon layer (23) with the oxidation barrier layer. (Column 2, line 57 – Column 3, line 47.)

Regarding claims 24 and 25, referencing Figures 4A-4E, Chen et al. further discloses thermally treating the target substrate (20) having the gate pattern with the oxidation barrier layer (29) in an oxygen-enriched environment. (Column 4, lines 8-17.)

Allowable Subject Matter

Claims 2, 5, 6, 8, 9 and 19-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Remmon R. Fordé whose telephone number is (571) 272-1916. The examiner can normally be reached on Monday-Thursday (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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